What is claimed is:

1. A timing circuit for use with transport logic in a network element, the network element forms part of a data network, the timing circuit comprising:

a timing receiver having a timing input, a timing output, and a selection input, the timing receiver operable to receive one or more timing signals at the timing input and to select a selected timing signal for distribution to the transport logic via the timing output based on a selection signal received at the selection input;

a determination circuit operable to determine whether the timing circuit is one of a master timing circuit and slave timing circuit, and based on the determination, produce the selection signal; and

a sync transmitter coupled to the timing output, the determination circuit, and a communication channel, the sync transmitter operable to receive the selected timing signal and to transmit the selected timing signal on the communication channel when the determination circuit determines that the timing circuit is the master timing circuit.

2. The timing circuit of claim 1, wherein the one or more timing signals include a client synchronization signal associated with client data that is to be transported on the data network.

3. The timing circuit of claim 2, wherein when the determination circuit determines that the timing circuit is the master timing circuit, the selection signal is generated to select the client synchronization signal associated with client data for distribution to the transport logic.

4. The timing circuit of claim 1, wherein the timing receiver is coupled to the communication channel and the one or more timing signals include a master sync signal received on the communication channel.

5. The timing circuit of claim 4, wherein when the determination circuit determines that the timing circuit is the slave timing circuit, the selection signal is generated to select the master sync signal for distribution to the transport logic.

6. The timing circuit of claim 1, wherein the one or more timing signals includes an external sync signal provide at the network element.

7. The timing circuit of claim 1, wherein the determination circuit is coupled to a message bus and is operable to receive at least one message over the message but to determine whether the timing circuit is one of the master timing circuit and the slave timing circuit.

8. The timing circuit of claim 1, wherein the determination circuit is operable to receive at least one local parameter to determine whether the timing circuit is one of the master timing circuit and the slave timing circuit.

9. A synchronization system for use in a network element that forms part of a data network, the network element includes transport logic to transport one or more data streams in the data network, wherein each of the one or more data streams has an associated synchronization signal, and wherein the transport logic comprises two or more circuit assemblies that are coupled together via a communication channel, the synchronization system comprising:

two or more determination circuits located on the two or more circuit assemblies, one determination circuit per circuit assembly, wherein each determination circuit includes logic to determine whether its respective circuit assembly is one of a master circuit assembly and a slave circuit assembly; and

two or more timing circuits coupled to the two or more determination circuits, one timing circuit per determination circuit, wherein each timing circuit includes logic to receive a plurality of synchronization signals and logic to selectively transmit a selected synchronization signal of the plurality of synchronization signals over the communication channel.

10. The synchronization system of claim 9, wherein the plurality of synchronization signals include the associated synchronization signals associated with the data streams to be transported in the data network.

11. The synchronization system of claim 10, wherein when a selected

determination circuit determines that its respective circuit assembly is the master circuit assembly, the timing circuit coupled to the selected determination circuit selects one of the associated synchronization signals as the selected synchronization signal and transmits the selected synchronization signal as a master sync signal over the communication channel.

12. The synchronization system of claim 9, wherein the plurality of synchronization signals include a master sync signal received over the communication channel.

13. The synchronization system of claim 12, wherein when a selected determination circuit determines that its respective circuit assembly is the slave circuit assembly, the timing circuit coupled to the selected determination circuit selects the master sync signal received over the communication channel and uses the master sync signal to synchronize its respective circuit assembly.

14. The synchronization system of claim 9, wherein the two or more determination circuits are coupled to a message bus and each determination circuit is operable to receive at least one message over the message to determine whether its respective circuit assembly is one of the master circuit assembly and the slave circuit assembly.

15. The synchronization system of claim 9, wherein each of the two or more determination circuit is operable to receive at least one local parameter to determine whether its respective circuit assembly is one of the master circuit assembly and the slave circuit assembly.

16. A synchronization system for use with an ADM card set in a network element that forms part of an optical network, the ADM card set comprising first and second circuit cards operable to transport data via the optical network, wherein the data has an associated synchronization signal, the synchronization system comprising:

a communication channel;

a determination circuit operable to determine which of the first and second circuit

cards is a master circuit card and which is a slave circuit card;

a first timing circuit located on the master circuit card and coupled to the communication channel, the first timing circuit includes logic to receive the associated synchronization signal and to synchronize the master circuit card to the associated synchronization signal, the first timing circuit further including logic to transmit the associated synchronization signal over the communication channel; and

a second timing circuit located on the slave circuit card and coupled to the communication channel, the second timing circuit having logic to receive the associated synchronization signal from the communication channel and to synchronize the slave circuit card to the associated synchronization signal.

17. The synchronization system of claim 16, wherein the determination circuit includes logic to determine which of the first and second circuit cards is the master circuit card and which is the slave circuit card by using a card position indicator associated with each card.

18. The synchronization system of claim 16, wherein the determination circuit comprises a first determination circuit coupled to the first timing circuit and a second determination circuit coupled to the second timing circuit, and wherein the first and second determination circuits are coupled to a message bus.

19. The synchronization system of claim 18, wherein the first and second determination circuits include logic to send at least one message over the message but to determine which of the first and second circuit cards is the master circuit card and which is the slave circuit card.

20. A method for synchronizing transport logic in a network element that forms part of a data network, the transport logic is used to transport one or more data streams in the data network, wherein each of the one or more data streams has an associated synchronization signal, and wherein the transport logic comprises two or more circuit assemblies that are coupled together via a communication channel, the method comprising steps of:

determining that a selected circuit assembly is a master circuit assembly and that

remaining circuit assemblies are slave circuit assemblies;

receiving at least one associated synchronization signal at the master circuit assembly;

synchronizing the master circuit assembly to the at least one associated synchronization signal;

distributing the at least one associated synchronization signal from the master circuit assembly to the slave circuit assemblies via the communication channel; and

synchronizing the slave circuit assemblies to the at least one associated synchronization signal.

21. The method of claim 20, wherein the step of determining comprises a step of determining that the selected circuit assembly is a master circuit assembly and that the remaining circuit assemblies are slave circuit assemblies using a position indicator associated with the respective circuit assembly.

22. The method of claim 20, wherein the communication channel includes a message bus and the step of determining comprises a step of determining that the selected circuit assembly is a master circuit assembly and that the remaining circuit assemblies are slave circuit assemblies using one or more messages transmitted over the message bus.

23. The method of claim 20, wherein the step of determining comprises a step of determining that the selected circuit assembly is a master circuit assembly and that the remaining circuit assemblies are slave circuit assemblies using at least one stored parameter.

24. The method of claim 20, wherein the transport logic is first transport logic and the one or more data streams are first client data streams, and wherein the network element includes second transport logic, the second transport logic is used to transport one or more second client data streams in the data network, wherein each of the one or more second client data streams has an associated synchronization signal, and wherein the second transport logic comprises two or more circuit assemblies that are coupled together via a second communication channel, the method comprising steps of:

determining that a selected circuit assembly of the second transport logic is a

second master circuit assembly and that remaining circuit assemblies of the second transport logic are second slave circuit assemblies;

receiving at least one associated synchronization signal associated with the second client data streams at the second master circuit assembly;

synchronizing the second master circuit assembly to the at least one associated synchronization signal associated with the second client data streams;

distributing the at least one associated synchronization signal associated with the second client data streams from the second master circuit assembly to the second slave circuit assemblies via the second communication channel; and

synchronizing the second slave circuit assemblies to the at least one associated synchronization signal associated with the second client data streams.